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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/690,434	10/18/2000	Masahisa Kobayashi	MA-448-US	3744
30743	7590 03/24/2004		EXAM	INER
WHITHAM, CURTIS & CHRISTOFFERSON, P.C.		CHANG, ERIC		
11491 SUNSE SUITE 340	ET HILLS ROAD		ART UNIT	PAPER NUMBER
RESTON, VA	A 20190		2116	8
			DATE MAILED: 03/24/2004	<b>.</b>

Please find below and/or attached an Office communication concerning this application or proceeding.

		Application No.	Applicant(s)	
		09/690,434	KOBAYASHI, MA	SAHISA
	Office Action Summary	Examiner	Art Unit	
		Eric Chang	2116	
Period fo	The MAILING DATE of this communication app or Reply	ears on the cover sheet	with the correspondence ad	ldress
THE - Exte after - If the - If NC - Failt Any earn	MAILING DATE OF THIS COMMUNICATION. maintains of time may be available under the provisions of 37 CFR 1.13 SIX (6) MONTHS from the mailing date of this communication. e period for reply specified above is less than thirty (30) days, a reply period for reply is specified above, the maximum statutory period we use to reply within the set or extended period for reply will, by statute, reply received by the Office later than three months after the mailing led patent term adjustment. See 37 CFR 1.704(b).	86(a). In no event, however, may within the statutory minimum of the statutory may be statutory minimum of the statuto	a reply be timely filed hirty (30) days will be considered timel DNTHS from the mailing date of this co ABANDONED (35 U.S.C. § 133).	
Status				
· —	Responsive to communication(s) filed on <u>30 De</u>			
	·—	action is non-final.		<del></del>
3)	Since this application is in condition for allowar closed in accordance with the practice under <i>E</i>	· ·	·	e ments is
	closed in accordance with the practice under L	x parte Quayle, 1955 C.	D. 11, 433 O.G. 213.	
Disposit	ion of Claims			
4)⊠	Claim(s) <u>1,3-16,18 and 19</u> is/are pending in the	e application.		
	4a) Of the above claim(s) is/are withdraw	vn from consideration.		
· · · · · ·	Claim(s) is/are allowed.			
	Claim(s) <u>1,3-16,18 and 19</u> is/are rejected.			
7)∐	Claim(s) is/are objected to.	e alaction rocuiromant		
8)[_	Claim(s) are subject to restriction and/or	election requirement.		
Applicat	ion Papers			
9)[	The specification is objected to by the Examiner	r.		
10)	The drawing(s) filed on is/are: a) acce	epted or b) objected to	by the Examiner.	
	Applicant may not request that any objection to the o	- ' '	• •	
4.00	Replacement drawing sheet(s) including the correcti	·		
11)[_]	The oath or declaration is objected to by the Ex-	aminer. Note the attach	ed Office Action or form PT	O-152.
Priority (	under 35 U.S.C. § 119			
· ·	Acknowledgment is made of a claim for foreign  ☐ All b)☐ Some * c)☐ None of:	priority under 35 U.S.C.	§ 119(a)-(d) or (f).	
	1. Certified copies of the priority documents	s have been received.		
	2. Certified copies of the priority documents			
	3. Copies of the certified copies of the prior		n received in this National	Stage
	application from the International Bureau		d as a stread	
- `	See the attached detailed Office action for a list of	or the certified copies no	it received.	

# Attachment(s)

1	N	Notice of	References	Cited (	PTO_892	١
ч,		Notice of	References	Citea	(F1O-092)	,

2) Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 5.

4) 📙	Interview Summary (PTO-413)
	Paper No(s)/Mail Date

5) Notice of Informal Patent Application (PTO-152)

6) 🔲 Other; \_\_\_\_.

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#### **DETAILED ACTION**

1. Claims 1, 3-16, 18 and 19 are pending.

### Response to Arguments

2. Applicant's arguments with respect to claims 1, 3-16, 18 and 19 have been considered but are most in view of the new ground(s) of rejection.

## Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

4. Claims 1, 3-16, 18 and 19 are rejected under 35 U.S.C. 102(e) as being clearly anticipated by U.S. Patent 6,351,818 to Murai.

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5. As to claim 1, Murai discloses a bus power-supply device for a node comprising a power-supply connection and a serial bus connection comprising a physical layer, wherein:

[a] when none of a power-supply voltage of said node is supplied, a DC voltage is supplied from the serial bus to a physical layer [col. 2, lines 24-27];

[b] when said power-supply voltage is supplied, a path for supplying the DC voltage from said serial bus is cut off [col. 2, lines 20-24];

[c] voltage detection means for detecting said power-supply voltage being supplied [col. 4, lines 58-66]; and

[d] selection means for supplying a DC voltage to a physical layer from said serial bus, and cutting off the path when the voltage detection means detects supply [col. 4, lines 58-66].

Murai teaches the physical layer switches between being exclusively self-powered by a local power-supply, and being bus-powered via a serial bus connection, depending on whether the local power-supply is available, substantially as claimed. Furthermore, Murai teaches that the path for supplying DC voltage from the serial bus is cut off when the node is powered by the local power-supply [col. 7, lines 58-67], and that the teachings are applied toward an IEEE 1394 Standard bus [col. 1, lines 5-7].

As to claims 3-7, 9-15 and 18, Murai discloses detecting whether power is being supplied by the power-supply by sampling the power-supply signal, and switching the access path to the serial bus voltage accordingly [FIG. 1-2]. Murai teaches there exists a path for supplying from the power-supply, and a path for supplying power from other devices via the serial bus,

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substantially as claimed, and Murai teaches that the second path is cut off when the voltage detection means detects supply. Furthermore, it would be well known to one of ordinary skill in the art to use a semiconductor switch or other like switch as the selection means [FIG 1, element 42], a comparator as a voltage detection means [FIG. 1, element 41], or a relay element as the voltage detection and selection means [FIG. 1, element 4], substantially as claimed.

- 7. As to claims 8 and 19, Murai discloses the power-supply device further comprising:
- [a] a power-supply circuit for providing DC voltage for the serial bus and physical layer of the node [FIG. 1, element 2];
- [b] selection means for supplying a DC voltage coming from said serial bus, and cutting off the path when the voltage detection means detects supply [col. 2, lines 14-17].
- 8. As to claim 16, Murai discloses a node connected to a serial bus, comprising a power-supply device comprising:
- [a] a plurality of connectors connected to the IEEE-1394 Standard serial bus for receiving voltage and other signals from other devices on the bus [col. 3, lines 34-56];
  - [b] a physical layer [FIG. 1, element 6];
  - [c] a bus power-supply device [FIG. 1, element 2]; wherein
- [d] when none of a power-supply voltage of said node is supplied, a DC voltage is supplied from the serial bus to a physical layer [col. 2, lines 24-27];
- [e] when said power-supply voltage is supplied, a path for supplying the DC voltage from said serial bus is cut off [col. 2, lines 20-24];

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[f] voltage detection means for detecting said power-supply voltage being supplied [col. 4, lines 58-66]; and

[g] selection means for supplying a DC voltage to a physical layer from said serial bus, and cutting off the path when the voltage detection means detects supply [col. 4, lines 58-66].

#### Conclusion

9. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eric Chang whose telephone number is (703) 305-4612. The examiner can normally be reached on M-F 9:00-5:30.

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If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas Lee can be reached on (703) 305-9717. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

March 12, 2004

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